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(54) **LOW-VOLTAGE, VERY-LOW-POWER CONDUCTANCE MODE NEURON**

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(56) **References Cited**

U.S. PATENT DOCUMENTS

4,956,564	9/1990	Holler et al.	307/201
4,961,002	10/1990	Tam et al.	395/24

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0 349 007   1/1990   (EP) .

OTHER PUBLICATIONS

Lee et al., "Analog Floating–Gate Synapses for General–Purpose VLSI Neural Computation," IEEE Transactions on Circuits and Systems, vol. 38, No. 6, pp. 654–658, Jun. 1991.*

White et al., "Electrically Modifiable Nonvolatile Synapses for Neural Networks," IEEE International Symposium on Circuits and Systems, vol. 2, pp. 1213–1216, May 1989.*

Mizugaki et al., "Implementation of New Superconducting Neural Circuits using Coupled SQUIDs," IEEE Transcriptions on Applied Superconductivity, vol. 4, No. 1, pp. 1–8, Mar. 1994.*

Kramer et al., "EEPROM Device as a Reconfigurable Analog Element for Neural Networks," International Electron Devices Meeting, 1989. Technical Digest, pp. 259–262, Dec. 1989.*

Sze, S.M., *Physics of Semiconductor Devices*, 2 ed., Wiley, 1981, p. 403.

(List continued on next page.)

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(57) **ABSTRACT**

A neural network including a number of synaptic weighting elements, and a neuron stage; each of the synaptic weighting elements having a respective synaptic input connection supplied with a respective input signal; and the neuron stage having inputs connected to the synaptic weighting elements, and being connected to an output of the neural network supplying a digital output signal. The accumulated weighted inputs are represented as conductances, and a conductance-mode neuron is used to apply nonlinearity and produce an output. The synaptic weighting elements are formed by memory cells programmable to different threshold voltage levels, so that each presents a respective programmable conductance; and the neuron stage provides for measuring conductance on the basis of the current through the memory cells, and for generating a binary output signal on the basis of the total conductance of the synaptic elements.

6 Claims, 8 Drawing Sheets
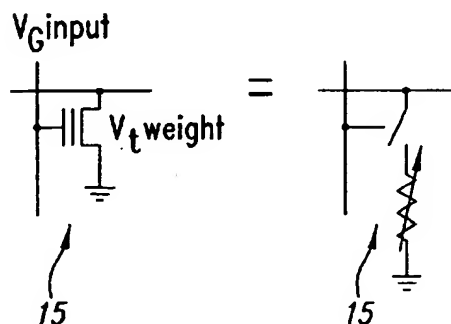
U.S. PATENT DOCUMENTS

4,988,891	1/1991	Mashiko	395/25
5,004,932	4/1991	Nejime	307/201
5,021,693	6/1991	Shima	327/357
5,021,988	6/1991	Mashiko	395/24
5,053,638	10/1991	Furutani et al.	395/24
5,056,037	10/1991	Eberhardt et al.	364/513
5,101,361 *	3/1992	Eberhardt	706/25
5,146,602	9/1992	Holler et al.	395/23
5,150,450 *	9/1992	Swenson et al.	706/25
5,155,377 *	10/1992	Castro	706/25
5,155,802	10/1992	Mueller et al.	395/24
5,187,680	2/1993	Engeler	364/807
5,202,956 *	4/1993	Mashiko	706/39
5,248,956 *	9/1993	Himes et al.	338/334
5,256,911	10/1993	Holler et al.	307/201
5,258,657 *	11/1993	Shibata et al.	326/35
5,268,320	12/1993	Holler et al.	438/591
5,274,746	12/1993	Mashiko	395/27
5,298,796	3/1994	Tawel	395/25
5,299,286 *	3/1994	Imondi et al.	706/37
5,305,250 *	4/1994	Salam et al.	708/801
5,336,937	8/1994	Sridhar et al.	395/24
5,343,555	8/1994	Yayla et al.	395/24
5,396,581	3/1995	Mashiko	395/24
5,422,982 *	6/1995	Pernisz	706/33
5,444,821	8/1995	Li et al.	395/24
5,475,794	12/1995	Mashiko	395/24
5,509,105	4/1996	Roenker et al.	395/24
5,615,305	3/1997	Nunally	395/24
5,704,014 *	12/1997	Marotta et al.	706/33
6,032,140 *	2/2000	Fabbrizio et al.	706/15

OTHER PUBLICATIONS

Jain, Jaswant R. and Anil K. Jain, "Displacement Measurement and Its Application in Interframe Image Coding," *IEEE Transactions on Communications* 29(12):1799–1808, Dec. 1981.

Degrauwe et al., "A Micropower CMOS–Instrumentation Amplifier," *IEEE J. of Solid–State Circuits* 20(3):805–807, Jun. 1985.

Sage et al., "An Artificial Neural Network Integrated Circuit Based on MNOS/CCD Principles," Proc. Conf. Neural Networks for Computing, J.S. Denker (ed.), Amer. Inst. of Physics, Snowbird, UT, 1986, pp. 381–385.

Graf et al., "A CMOS Associative Memory Chip," Proc. IEEE First International Conference Neural Networks, M. Caudill and C. Butler (ed.), SOS Printing, San Diego, CA, 1987, pp. III–461–III–468.

Seevinck, Evert and Roelof F. Wassenaar, "A Versatile CMOS Linear Transconductor/ Square–Law Function Circuit," *IEEE J. of Solid–State Circuits* 22(3):366–377, Jun. 1987.

Holler et al., "An Electrically Trainable Artificial Neural Network (ETANN) With 10240 'Floating Gate' Synapses," Proc. IJCNN, pp. 2.191–2.196, Jun. 1989.

Kramer et al., "EEPROM Device as a Reconfigurable Analog Element For Neural Networks," *IEDM Tech. Digest*, pp. 10.3.1–10.3.4, Dec. 1989.

Graf, Hans Peter and Don Henderson, "A Reconfigurable CMOS Neural Network," *IEEE ISSCC*, pp. 144–145, Feb. 1990.

Hollis, Paul W. and John J. Paulos, Artificial Neural Networks Using MOS Analog Multipliers, *IEE J. of Solid–State Circuits* 25(3):849–855, Jun. 1990.

Boser et al., "An Analog Neural Network Processor With Programmable Topology," *IEEE J. of Solid–State Circuits* 26(12):2017–2025, Dec. 1991.

Satyanarayana et al., A Reconfigurable VLSI Neural Network, *IEEE J. of Solid–State Circuits* 27(1):67–81, Jan. 1992.

Chandrakasan et al., "Low–Power CMOS Digital Design," *IEEE J. of Solid–State Circuits* 27(4):473–484, Apr. 1992.

Sin et al., "EEPROM as an Analog Storage Device, With Particular Applications in Neural Networks," *IEEE Transactions on Electron Devices* 39(6):1410–1419, Jun. 1992.

Tsukano et al., "A New CMOS Neuron Circuit Based on a Cross–Coupled Current Comparator Structure," *IEICE Transactions on Fundamentals of Electronics* E75–A(7):937–943, Jul. 1992.

Costto, E. and H.P. Graf, "NET32K High Speed Image Understanding System," Proc. Fourth International Conference on Microelectronics for Neural Networks and Fuzzy Systems, IEEE Computer Society Press, Los Alamitos, CA, 1994, pp. 413–421.

Guardiani et al., "Applying a submicron mismatch model to practical IC design," *Proc. of the CICC*, pp. 13.3.1–13.3.4, 1994.

Lazzaro et al., "Systems Technologies for Silicon Auditory Models," *IEEE Micro* 14(3): 7–15, Jun. 1994.

König et al., Massively Parallel VLSI–Implementation of a Dedicated Neural Network for Anomaly Detection in Automated Visual Quality Control, *Proc. Microneuro*, pp. 354–364, Sep. 1994.

Kramer et al., "Flash–Based Programmable Nonlinear Capacitor for Switched–Capacitor Implementations of Neural Networks," *IEDM Tech. Dig.*, pp. 17.6.1–17.6.4, Dec. 1994.

Kovács–V., Zsolt M. and Roberto Guerrieri, "Massively–Parallel Handwritten Character Recognition Based on the Distance Transform," *Pattern Recognition* 28(3):293–301, 1995.

Kramer et al., "Ultra–Low–Power Analog Associative Memory Core Using Flash–EEPROM–Based Programmable Capacitors," Proc. 1995 International Symposium on Low Power Design, Association for Computing Machinery, Dana Point, CA, 1995, pp. 203–208.

Fabbrizio et al., "Low Power, Low Voltage Conductance–Mode CMOS Analog Neuron," *Proc. of MicroNeuro*, pp. 111–115, 1996.

Tomasini et al., "B/W Adaptive Image With Analog Motion Vector Estimator at 0.3GOPS," *ISSCC Dig. Of Tech Papers*, pp. 94–95, 425, 1996.

Fabbrizio et al., "Low Power, Low Voltage Conductance–Mode CMOS Analog Neuron," *Proc. of MicroNeuro '96*, pp. 111–115, Feb. 1996.

Benson et al., "UV–Activated Conductances Allow for Multiple Time Scale Learning," IEEE Transactions on Neural Networks, vol. 4, No. 3, pp. 434–440, May 1993.

* cited by examiner